

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	1	"20020138244"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2008/01/05 14:51
L12	0	(IP adj core) with obfuscation\$4 same (simulat\$4 model\$4 design\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/05 15:00
L13	12	((IP adj core) hdl vhdl verilog hardware) with obfuscation\$4 same (simulat\$4 model\$4 design\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/05 14:53
L14	0	(IP adj core) with ((add\$3 appl\$4) with (encrypt\$4 obfuscation\$4)) same (simulat\$4 model\$4 design\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/05 15:02
L15	0	(IP adj core) same ((add\$3 appl\$4) with (encrypt\$4 obfuscation\$4)) same (simulat\$4 model\$4 design\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/05 15:02
L16	145	((IP adj core) hdl vhdl verilog hardware FPGA PLD) same ((add\$3 appl\$4) with (encrypt\$4 obfuscation\$4)) same (simulat\$4 model\$4 design\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/05 15:05
L17	8	((IP adj core) hdl vhdl verilog hardware FPGA PLD) same ((add\$3 appl\$4) with (obfuscation\$4)) same (simulat\$4 model\$4 design\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/01/05 15:03
L18	10	((5,381,347) or (5,646,651) or (5, 731,811) or (5,825,879) or (5,881, 287) or (5,936,616) or (5,961, 617) or (6,209,103) or (6,298, 446) or (6353,892)).PN.	USPAT; USOCR	OR	OFF	2008/01/05 15:06
L19	1	(7107567).PN.	USPAT; USOCR	OR	OFF	2008/01/05 15:16
L20	5	(20030188275 20040088674 20050071792 6539525).PN. OR (7107567).URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/05 15:17

Google[Advanced Search](#)[Preferences](#)**Web**Results 1 - 10 of about 44 for **"IP core" "obfuscation" "simulation"**. (0.14 seconds)**[PDF] Microsoft PowerPoint - cs6812_Seminar_3_JHDL.ppt**File Format: PDF/Adobe Acrobat - [View as HTML](#)Provides **simulation** and evaluation of circuits over the ... Changes to a proprietary bit stream enable the **IP core** to be hidden. from the user ...www.arl.wustl.edu/~lockwood/class/cs6812/cs6812_Seminar_3_JHDL.pdf - [Similar pages](#)**Electronic design protection circuit - US Patent 7107567**Because the **simulation** version of an **IP core** must work with a variety of ... For example, during **obfuscation**, clues for understanding the model (for example ...www.patentstorm.us/patents/7107567-description.html - 88k - [Cached](#) - [Similar pages](#)**IP delivery for FPGAs using applets and JHDL - Design Automation ...**class file **obfuscation** and class encryption may be added to. increase the security of the **IP**. ... **IP-core** analysis and **simulation**. In. Proceedings ...ieeexplore.ieee.org/iel5/7910/21813/01012584.pdf - [Similar pages](#)**[PDF] Cyber infrastructure**File Format: PDF/Adobe Acrobat - [View as HTML](#)research supports software protection with **obfuscation** and ... The **IP core** protection problem in. this domain, analogous to software protection, ...www.ece.iastate.edu/fileadmin/www.ece.iastate.edu/images/research_documents/cyber-infrastructure2007.pdf - [Similar pages](#)**VHDL Issue Number: 2024 Language Version: VHDL-2002 Classification ...**... code encryption or **obfuscation** should be built into the VHDL standard. ... part of our **IP core** deliverables to customers, we normally provide **simulation** ...www.eda-stds.org/isac/IRs-VHDL-2002/IR2024.txt - 3k - [Cached](#) - [Similar pages](#)**FPGA FAQ comp.arch.fpga archives - messages from 65600**The design basically consists of a 3rd party **IP core**, for > which I don't have a source (IThank you > Giuseppe Eschew **obfuscation**! Bob Article: 65619 ...www.fpga-faq.com/archives/65600.html - 68k - [Cached](#) - [Similar pages](#)**UCLA General Catalog 2007-08: Computer Science Course Listings**Introduction to methods for modeling and **simulation** using interactive lower bounds on use of cryptographic primitives, software **obfuscation**. ...www.registrar.ucla.edu/Catalog/catalog07-08-2011.html - 93k - [Cached](#) - [Similar pages](#)**VLSI CAD tool protection by birthmarking design solutions**... tamper-proofing, and **obfuscation**--tools for software protection", ... "A Web-CADMethodology for **IP-Core** Analysis and **Simulation**", DAC 00, pp. 597--600. ...portal.acm.org/citation.cfm?id=1057661.1057743 - [Similar pages](#)**Conference Papers**Yu Yu, Jussipekka Leiwo & Benjamin Premkumar, "Program **Obfuscation** via J. Gu, C.H. Chang and K. S. Yeo, "An area and energy efficient **IP core** for ...www.chipes.ntu.edu.sg/contents/library/ConferencePapers.htm - 104k -[Cached](#) - [Similar pages](#)

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